Ideal Op Amp Circuits

The operational amplifier, or op amp as it is commonly called, is a fundamental active element of analog circuit design. It is most commonly used in amplifier and analog signal processing circuits in the frequency band from 0 to 100 kHz. High-frequency op amps are used in applications that require a bandwidth into the MHz range. The first op amps were vacuum-tube circuits which were developed for use in analog computers. Modern op amps are fabricated as integrated circuits that bear little resemblance to the early circuits. This chapter covers some of the basic applications of the op amp. It is treated as an ideal circuit element without regard to its internal circuitry. Some of the limitations imposed by non-ideal characteristics are covered in the following chapter.

The notation used here is as follows: Total quantities are indicated by lower-case letters with upper-case subscripts, e.g. $v_I$, $i_O$, $r_{IN}$. Small-signal quantities are indicated by lower-case letters with lower-case subscripts, e.g. $v_i$, $i_o$, $r_{out}$. Transfer function variables and phasors are indicated by upper case letters and lower-case subscripts, e.g. $V_i$, $I_o$, $Z_{in}$.

1.1 The Ideal Op Amp

The ideal op amp is a three terminal circuit element that is modeled as a voltage-controlled voltage source. That is, its output voltage is a gain multiplied by its input voltage. The circuit symbol for the ideal op amp is given in Fig. 1.1(a). The input voltage is the difference voltage between the two input terminals. The output voltage is measured with respect to the circuit ground node. The model equation for the output voltage is

$$v_O = A (v_+ - v_-)$$

where $A$ is the voltage gain, $v_+$ is the voltage at the non-inverting input, and $v_-$ is the voltage at the inverting input. The controlled source model of the ideal op amp is shown in Fig. 1.1(b).

![Figure 1.1: (a) Op-amp symbol. (b) Controlled-source model.](image-url)

The terminal characteristics of the ideal op amp satisfy four conditions. These are as follows:

1. The current in each input lead is zero.
2. The output voltage is independent of the output current.
3. The voltage gain $A$ is independent of frequency.

4. The voltage gain $A$ is very large, approaching infinity in the limit.

The first condition implies that the resistance seen looking into both input terminals is infinite. The second implies that the voltage gain is independent of the output current. This is equivalent to the condition that the output resistance is zero. The third implies that the bandwidth is infinite. The fourth implies that the difference voltage between the two input terminals must approach zero if the output voltage is finite.

For it to act as an amplifier, the op amp must have feedback applied from its output to its inverting input. That is, part of the output voltage must be sampled by a network and fed back into the inverting input. This makes it possible to design an amplifier so that its gain is controlled by the feedback network.

To illustrate how feedback affects the op amp, consider the circuits shown in Fig. 1.2. The networks labeled $N_1$ and $N_F$, respectively, are the input and feedback networks. The op amp of Fig. 1.2(a) has positive feedback whereas the op amp of Fig. 1.2(b) has negative feedback. Let a unit step of voltage be applied to the input of each circuit at $t = 0$. The arrows in the figures indicate the directions in which the input voltages change, i.e. each input voltage increases. For the circuit of Fig. 1.2(a), the voltage increase at $v_i$ is fed through the $N_1$ network to cause the voltage to increase at the $v_+$ terminal. This is amplified by a positive gain ($+A$) and causes the output voltage to increase. This is fed back through the $N_F$ network to further increase the voltage at the $v_+$ terminal. (The arrow for the feedback voltage is enclosed in parentheses to distinguish it from the arrow for the initial increase in voltage.) This causes the output voltage to increase further, causing $v_+$ to increase further, etc. It follows that the circuit is not stable with positive feedback.

For the circuit of Fig. 1.2(b), the voltage increase at the input is fed through the $N_1$ network to cause the voltage to increase at the $v_-$ terminal. This is amplified by a negative gain ($-A$) and causes the output voltage to decrease. This is fed back through the $N_F$ network to cause the voltage at the $v_-$ input to decrease, thus tending to cancel the initial increase caused by the input voltage. Because the $v_-$ voltage is decreased by the feedback, it follows that $v_o$ is decreased also. Thus the circuit is stable.

When negative feedback is used in an op amp circuit, the feedback tends to force the voltage at the $v_-$ input to be equal to the voltage at the $v_+$ input. It is said that a virtual short circuit exists between the two inputs. A virtual short circuit between two nodes means that the voltage difference between the nodes is zero but there is no branch for a current to flow between the nodes. There is no virtual short circuit between the $v_-$ and $v_+$ inputs to an op amp which has positive feedback. If it has both negative and positive feedback, the virtual short circuit exists if the negative feedback is greater than the positive feedback.

We have used the concept of signal tracing in the circuits of Fig. 1.2 to illustrate the effects of feedback. Signal tracing is a simple concept which can be applied to any circuit to check for positive and negative feedback. Circuits which have positive feedback are unstable in general and are not used for amplifier circuits. With few exceptions, the circuits covered in this chapter have only negative feedback.
1.2 Inverting Amplifiers

1.2.1 The Inverting Amplifier

Figure 1.3(a) shows the circuit diagram of an inverting amplifier. The input signal is applied through resistor $R_1$ to the inverting op amp input. Resistor $R_F$ is the feedback resistor which connects from the output to the inverting input. The circuit is called an inverting amplifier because its voltage gain is negative. This means that if the input voltage is increasing or going positive, the output voltage will be decreasing or going negative, and vice versa. The non-inverting input to the op amp is not used in the inverting amplifier circuit. The figure shows this input grounded so that $v_+ = 0$.

![Circuit Diagram](image_url)

For the circuit of Fig. 1.3(a), the voltage at the inverting input is given by $v_- = -v_O/A$. For $v_O$ finite and $A \to \infty$, it follows that $v_- \to 0$. Even though the $v_-$ input is not grounded, it is said to be a virtual ground because the voltage is zero, i.e. at ground potential. Because $i_- = 0$, the sum of the currents into the $v_-$ node through resistors $R_1$ and $R_F$ must be zero, i.e. $i_1 + i_F = 0$, where $i_1 = v_I/R_1$ and $i_F = v_O/R_F$. Thus we can write

$$i_1 + i_F = 0 \implies \frac{v_I}{R_1} + \frac{v_O}{R_F} = 0 \quad (1.2)$$

This relation can be solved for the voltage gain to obtain

$$\frac{v_O}{v_I} = -\frac{R_F}{R_1} \quad (1.3)$$

The input resistance is calculated from the relation $r_{in} = v_I/i_1$. Because $v_- = 0$, it follows that

$$r_{in} = R_1 \quad (1.4)$$

The output resistance is equal to the output resistance of the op amp so that

$$r_{out} = 0 \quad (1.5)$$

The controlled source model of the inverting amplifier is shown in Fig. 1.3(b).

Example 1 Design an inverting amplifier with an input resistance of 2 kΩ, an output resistance of 100 Ω, and an open-circuit voltage gain of $-30$ (an inverting decibel gain of 29.5 dB).

Solution. The circuit diagram for the amplifier is given in Fig. 1.4(a). For an input resistance of 2 kΩ, Eq. (1.4) gives $R_1 = 2$ kΩ. For a voltage gain of $-30$, it follows from Eq. (1.3) that $R_F = 60$ kΩ. For an output resistance of 100 Ω, the resistor $R_O = 100$ Ω must be used in series with the output as shown in the figure.

Example 2 Calculate the voltage gain of the circuit of Fig. 1.4(a) if a 1 kΩ load resistor is connected from the output to ground. The circuit with the load resistor is shown in Fig. 1.4(b).
Solution. The voltage gain decreases when $R_L$ is added because of the voltage drop across $R_O$. By voltage division, the gain decreases by the factor

$$\frac{R_L}{R_O + R_L} = \frac{1000}{1000 + 100} = \frac{10}{11}$$

It follows that the loaded voltage gain is $(10/11) \times (-30) = -27.3$ (an inverting decibel gain of 28.7 dB).

**Example 3** For the inverting amplifier circuit of Fig. 1.4(b), investigate the effect of connecting the feedback resistor $R_F$ to the load resistor $R_L$ rather than to the op amp output terminal. The modified circuit is shown in Fig. 1.4(c).

Solution. Because $i_1 + i_F = 0$, it follows that $v_I/R_1 + v_O/R_F = 0$. This gives the voltage gain $v_O/v_I = -R_F/R_1$. Because this is independent of $R_L$, it follows that the output resistance of the circuit is zero. Thus the circuit looks like the original circuit of Fig. 1.4(b) with $R_O = 0$. With $R_O \neq 0$, the op amp must put out a larger voltage in order to maintain a load voltage that is independent of $R_O$. Let $v'_O$ be the voltage at the op amp output terminal in Fig. 1.4(c). By voltage division, the output voltage is given by

$$\frac{v_O}{v'_O} = \frac{R_L}{R_L || R_F}$$

It follows that $v'_O$ is larger than $v_O$ by the factor $1 + R_O/(R_L || R_F)$. Because this is greater than unity, $R_O$ causes the op amp to “work harder” to put out a larger output voltage. We conclude that a resistor should not be connected in series between the op amp output terminal and the connection for the feedback resistor.

**1.2.2 The Inverting Amplifier with T Feedback Network**

If a high voltage gain is required from an inverting amplifier, Eq. (1.3) shows that either $R_F$ must be large, $R_1$ must be small, or both. If $R_1$ is small, the input resistance given by Eq. (1.4) may be too low to meet specifications. The inverting amplifier with a T feedback network shown in Fig. 1.5(a) can be used to obtain a high voltage gain without a small value for $R_1$ or very large values for the feedback resistors.
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Figure 1.5: (a) Inverting amplifier with a T feedback network. (b) Equivalent circuit for calculating \( v_O \).

The solution for the voltage gain is simplified by making a Thévenin equivalent circuit at the \( v_- \) terminal looking to the right through \( R_2 \). The circuit is given in Fig. 1.5(b). Because \( i_1 + i_F = 0 \), it follows that

\[
\frac{v_I}{R_1} + \frac{v_O R_3}{R_3 + R_4} \times \frac{1}{R_2 + R_3||R_4} = 0
\]

This equation can be solved for the voltage gain to obtain

\[
\frac{v_O}{v_I} = -\left[ \frac{R_2}{R_1} + \frac{R_1}{R_1} \left( 1 + \frac{R_2}{R_3} \right) \right]^{-1}
\]

The output resistance of the circuit is zero. The input resistance is \( R_1 \).

**Example 4** For the inverting amplifier with a T feedback network in Fig. 1.5(a), specify the resistor values which give an input resistance of 10 kΩ and a gain of \(-100\). The maximum resistor value in the circuit is limited to 100 kΩ.

Solution. To meet the input resistance specification, we have \( R_1 = 10 \) kΩ. Let \( R_2 = R_4 = 100 \) kΩ. It follows from Eq. (1.7) that \( R_3 \) is given by

\[
R_3 = \frac{R_2 R_4}{(-v_O/v_I) R_1 - (R_2 + R_4)}
\]

This equation gives \( R_3 = 12.5 \) kΩ.

1.2.3 The Current-to-Voltage Converter

The circuit diagram of a current-to-voltage converter is shown in Fig. 1.6(a). The circuit is a special case of an inverting amplifier where the input resistor is replaced with a short circuit. Because the \( v_- \) terminal is a virtual ground, the input resistance is zero. The output resistance is also zero. Because \( i_1 + i_F = 0 \) and \( v_O = i_F R_F \), it follows that the transresistance gain is given by

\[
\frac{v_O}{i_1} = -R_F
\]

Figure 1.6(b) shows the current-to-voltage converter with a current source connected to its input. Because \( R_S \) connects from a virtual ground to ground, the current through \( R_S \) is zero. It follows that \( i_1 = i_S \) and \( v_O = -R_F i_S \). Thus the output voltage is independent of \( R_S \).
1.3 Non-Inverting Amplifiers

1.3.1 The Non-Inverting Amplifier

Figure 1.7(a) shows the circuit diagram of a non-inverting amplifier. The input voltage $v_I$ is applied to the non-inverting op amp input. A voltage divider consisting of resistors $R_F$ and $R_1$ connects from the output node to the inverting input. The circuit is called a non-inverting amplifier because its voltage gain is positive. This means that if the input voltage is increasing or going positive, the output voltage will also be increasing or going positive. If the circuit diagrams of the inverting and the non-inverting amplifiers are compared, it can be seen that the circuits are the same if $v_I = 0$. Thus the only difference between the two circuits is the node at which the input voltage is applied.

For the circuit of Fig. 1.7(a), the voltage difference between the two op amp input terminals is given by $v_+ - v_- = v_O/A$. For $v_O$ finite and $A \to \infty$, it follows that $v_+ \to v_-$. It is said that a virtual short circuit exists between the two inputs because there is no voltage difference between the two terminals. For $i_- = 0$, the condition that $v_+ = v_-$ requires $v_I$ and $v_O$ to satisfy the equation

$$v_+ = v_- \implies v_I = v_O \frac{R_1}{R_F + R_1}$$ \hspace{1cm} (1.9)

where voltage division has been used for $v_-$. This can be solved for the voltage gain to obtain

$$\frac{v_O}{v_I} = 1 + \frac{R_F}{R_1}$$ \hspace{1cm} (1.10)

The input and output resistances are given by

$$r_{in} = \infty$$ \hspace{1cm} (1.11)
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\[ r_{out} = 0 \]  
\[(1.12)\]

The controlled source model for the non-inverting amplifier is shown in Fig. 1.7(b).

**Example 5** Design a non-inverting amplifier which has an input resistance of 10 kΩ, an open-circuit voltage gain of 20 (a decibel voltage gain of 26 dB), and an output resistance of 600 Ω. The feedback network is specified to draw no more than 0.1 mA from the output of the op amp when the open-circuit output voltage is in the range \(-10 \text{ V} \leq v_O \leq 10 \text{ V}\).

**Solution.** The circuit diagram for the amplifier is shown in Fig. 1.8. To meet the input resistance specification, we have \(R_i = 10 \text{ kΩ}\). For the specified current in the feedback network, we must have \(0.1 \text{ mA} \leq 10/(R_F + R_1)\). If the equality is used, we obtain \(R_F + R_1 = 100 \text{ kΩ}\). For the specified open-circuit voltage gain, Eq. (1.10) gives \(1 + R_F/R_1 = 20\) or \(R_F = 19R_1\). It follows that \(R_1 = 5 \text{ kΩ}\) and \(R_F = 95 \text{ kΩ}\). To meet the output resistance specification, we must have \(R_O = 600 \text{ Ω}\).

![Figure 1.8: Circuit for Example 5.](image)

**Example 6** Examine the effect of connecting a resistor between the \(v_+\) node and the \(v_-\) node in the non-inverting amplifier of the circuit for Example 5.

**Solution.** For an ideal op amp, the voltage difference between the \(v_+\) and \(v_-\) terminals is zero. It follows that a resistor connected between these nodes has no current flowing through it. Therefore, the resistor has no apparent effect on the circuit. This conclusion applies also for the inverting amplifier circuit of Fig. 1.3. With physical op amps, however, a resistor connected between the \(v_+\) and the \(v_-\) terminals can affect the performance of the circuit by reducing the effective open-loop gain \(A\).

### 1.3.2 The Voltage Follower

The voltage follower or unity-gain buffer is a unity-gain non-inverting amplifier. The circuit diagram is shown in Fig. 1.9(a). Compared to the non-inverting amplifier of Fig. 1.7(a), the feedback resistor \(R_F\) is replaced by a short circuit and resistor \(R_1\) is omitted. Because the output node is connected directly to the inverting input instead of through a voltage divider, the circuit is said to have 100% feedback. Because \(v_+ = v_-\), it follows that \(v_O = v_I\). Therefore, the circuit has unity voltage gain. The voltage follower is often used to isolate a low resistance load from a high output resistance source. That is, the voltage follower supplies the current to drive the load while drawing no current from the input circuit.

**Example 7** Figure 1.9(b) shows a source connected to a load with a voltage follower. It is given that \(R_S = 10 \text{ kΩ}\) and \(R_L = 100 \text{ Ω}\). (a) Calculate \(v_O\). (b) Calculate \(v_O\) if the voltage follower is removed and the source connected to the load.

**Solution.** (a) With the voltage follower, there is no current through \(R_S\) so that the voltage at the op amp input is \(v_S\). It follows that \(v_O = v_S\). (b) If the voltage follower is removed and the source is connected directly to the load, \(v_O\) is given by \(v_O = v_SR_L/(R_S + R_L) = v_S/101\). This is a decrease in output of 20 log 101 = 40.1 dB. This example illustrates how a unity gain amplifier can increase the gain of a circuit.
1.3.3 Amplifier with Voltage and Current Feedback

Figure 1.10(a) shows the circuit diagram of a non-inverting amplifier in which the voltage fed back to the inverting input of the op amp is a function of both the load voltage and the load current. To solve for the output voltage, it is convenient to first form the Thévenin equivalent circuit seen by the load resistor $R_L$. The circuit is shown in Fig. 1.10(b). It consists of a voltage source in series with a resistor. The voltage source has a value equal to the open-circuit load voltage, i.e. the output voltage with $R_L \to \infty$. The resistor has a value equal to the ratio of the open-circuit load voltage to the short-circuit load current, i.e. the output current with $R_L = 0$.

With $R_L = \infty$, the open-circuit load voltage is given by $v_{O(oc)} = i_1 (R_F + R_1)$. Because there is a virtual short circuit between the $v_+$ and the $v_-$ terminals, it follows that $i_1 = v_I / (R_1 + R_2)$. It follows that $v_{O(oc)}$ can be written

$$v_{O(oc)} = v_I \frac{R_1 + R_F}{R_1 + R_2} \quad (1.13)$$

With $R_L = 0$, there can be no current through $R_F$ or $R_1$ so that $v_I = v_- = i_{O(sc)} R_2$. Thus $i_{O(sc)}$ is given by

$$i_{O(sc)} = \frac{v_I}{R_2} \quad (1.14)$$

The output resistance of the circuit is given by

$$r_{out} = \frac{v_{O(oc)}}{i_{O(sc)}} = \frac{R_2 R_1 + R_F}{R_1 + R_2} \quad (1.15)$$

By voltage division, it follows from Fig. 1.10(b) and Eq. (1.13) that the output voltage can be written

$$v_O = v_{O(oc)} \times \frac{R_L}{r_{out} + R_L} = v_I \frac{R_1 + R_F}{R_1 + R_2} \times \frac{R_L}{r_{out} + R_L} \quad (1.16)$$
1.3.4 The Negative Impedance Converter

Although it is not an amplifier, the negative impedance converter is an application of the non-inverting configuration. For the circuit in Fig. 1.11(a), the resistor $R$ bridges the input and output terminals of a non-inverting amplifier. We can write

$$r_{in} = \frac{v_I}{i_1}$$  \hspace{1cm} (1.17)

$$i_1 = \frac{v_I - v_O}{R}$$  \hspace{1cm} (1.18)

$$v_O = \left(1 + \frac{R_F}{R_1}\right)v_I$$  \hspace{1cm} (1.19)

Solution for $r_{in}$ yields

$$r_{in} = -\frac{R_1}{R_F}R$$  \hspace{1cm} (1.20)

Thus the circuit has a negative input resistance.

![Negative Impedance Converter Diagram](image)

Figure 1.11: Negative impedance converters. (a) Negative input resistance. (b) Negative input capacitance.

A resistor in parallel with another resistor equal to its negative is an open circuit. It follows that the output resistance of a non-ideal current source, i.e. one having a non-infinite output resistance, can be made infinite by adding a negative resistance in parallel with the current source. Negative resistors do not absorb power from a circuit. Instead, they supply power. For example, if a capacitor with an initial voltage on it is connected in parallel with a negative resistor, the voltage on the capacitor will increase with time. Relaxation oscillators are waveform generator circuits which use a negative resistance in parallel with a capacitor to generate ac waveforms.

The resistor is replaced with a capacitor in Fig. 1.11(b). In this case, the input impedance is

$$Z_{in} = -\frac{R_1}{R_F} \left(\frac{1}{j\omega C}\right) = j\omega \frac{R_1}{\omega^2 R_F C} = j\omega L_{eq}$$  \hspace{1cm} (1.21)

It follows that the input impedance is that of a frequency dependent inductor given by

$$L_{eq} = \frac{R_1}{\omega^2 R_F C}$$  \hspace{1cm} (1.22)

1.4 Summing Amplifiers

1.4.1 The Inverting Summer

The inverting summer is the basic op amp circuit that is used to sum two or more signal voltages, to sum a dc voltage with a signal voltage, etc. An inverting summer with four inputs is shown in Fig. 1.12(a). If all
inputs are grounded except the $v_{Ij}$ input, where $j = 1, 2, 3, o r 4$, Eq. (1.3) for the inverting amplifier can be used to write $v_O = -(R_F/R_j)v_{Ij}$. It follows by superposition that the total output voltage is given by

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} - \frac{R_F}{R_3}v_{I3} - \frac{R_F}{R_4}v_{I4}$$  \hspace{1cm} (1.23)

The input resistance to the $j$th input is $R_j$. The output resistance of the circuit is zero.

![Diagram](image)

Figure 1.12: (a) Four input inverting summer. (b) Circuit for Example 8.

**Example 8** Design an inverting summer which has an output voltage given by

$$v_O = 3 - 2v_I$$

Assume that $+15$ V and $-15$ V supply voltages are available.

**Solution.** The output contains a dc term of +3 V. This can be realized by using the $-15$ V supply as one input. The circuit is shown in Fig. 1.12(b). For the specified output, we can write $(-15) \times (-R_F/R_1) = 3$ and $-R_F/R_2 = -2$. If $R_F$ is chosen to be $3\, \text{k}\Omega$, it follows that $R_1 = 15\, \text{k}\Omega$ and $R_2 = 1.5\, \text{k}\Omega$.

### 1.4.2 The Non-Inverting Summer

A non-inverting summer can be realized by connecting the inputs through resistors to the input terminal of a non-inverting amplifier. Unlike the inverting amplifier, however, the input resistors do not connect to a virtual ground. Thus a current flows in each input resistor that is a function of the voltage at all inputs. This makes it impossible to define the input resistance for any one input unless all other inputs are grounded. The circuit diagram for a four-input non-inverting summer is shown in Fig. 1.13(a). To solve for the output voltage, it is convenient to first make Norton equivalent circuits at the $v_+$ terminal for each of the inputs. The circuit is shown in Fig. 1.13(b).

Eq. (1.10) can be used to write the equation for $v_O$ as follows:

$$v_O = v_+ \left(1 + \frac{R_F}{R_6}\right)$$

$$= \left(\frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \frac{v_{I3}}{R_3} + \frac{v_{I4}}{R_4}\right) \left(R_1 \parallel R_2 \parallel R_3 \parallel R_4 \parallel R_5\right) \left(1 + \frac{R_F}{R_6}\right)$$  \hspace{1cm} (1.24)

The output resistance of the circuit is zero. If the $v_{I2}$ through $v_{I4}$ inputs are grounded, the input resistance to the $v_{I1}$ node is given by

$$r_{in1} = R_1 + R_2 \parallel R_3 \parallel R_4 \parallel R_5$$  \hspace{1cm} (1.25)

The input resistance to the other inputs can be written similarly.
1.4. SUMMING AMPLIFIERS

Example 9  Design a two-input non-inverting summer which has an output voltage given by

\[ v_O = 8(v_{I1} + v_{I2}) \]

With either input grounded, the input resistance to the other input terminal is specified to be 10 kΩ. In addition, the current which flows in the grounded input lead is to be 1/10 the current that flows in the ungrounded lead.

Solution. The circuit is shown in Fig. 1.14. By symmetry, it follows that \( R_2 = R_1 \). For the input resistance specification, we must have \( R_1 + R_1 || R_3 = 10 \text{kΩ} \). If \( v_{I2} \) is grounded, \( i_2 = -i_1 R_3 / (R_3 + R_1) \). For \( i_2 = -i_1 / 10 \), we have \( R_3 / (R_3 + R_1) = 1/10 \). It follows from these two equations that \( R_3 = 10/9.9 \text{kΩ} = 1.01 \text{kΩ} \) and \( R_1 = R_2 = 9R_3 = (10/1.1) \text{kΩ} = 9.09 \text{kΩ} \).

If \( v_{I1} = v_{I2} = v_I \), it follows that \( v_O/v_I = 16 \). Thus we can write the design equation

\[ 16 = \frac{v_O}{v_I} \times \frac{v_O}{v_+} = \frac{R_3}{R_3 + R_1/2} \left( 1 + \frac{R_F}{R_4} \right) \]

It follows from this equation that \( 1 + R_F/R_4 = 88 \). This can be achieved with \( R_4 = 270 \text{Ω} \) and \( R_F = 23.5 \text{kΩ} \).
From Eq. (1.65), it follows that the input impedance circuit consists of a $1000 \Omega$ resistor to ground in parallel with a negative inductor to ground having the value $-1000^2 \times 10^{-6} = -1 \text{H}$.

### 1.8 Low-Pass Amplifiers

#### 1.8.1 The Inverting Low-Pass Amplifier

This section covers several of the many op amp circuits which have a voltage gain transfer function that is of the form of single-pole low-pass and low-pass shelving transfer functions. Fig. 1.28(a) shows the circuit of an inverting low-pass amplifier. The voltage gain is obtained from Eq. (1.3) by replacing $R_F$ with $R_F\|(1/C_F s)$. It is given by

$$
\frac{V_o}{V_i} = -\frac{R_F}{R_1}\left(1/C_F s\right) = -\frac{R_F}{R_1} \times \frac{1}{1 + R_F C_F s}
$$

(1.66)

This is of the form of a gain constant $-R_F/R_1$ multiplied by a low-pass transfer function having a pole time constant $R_F C_F$. The Bode magnitude plot for the transfer function is given in Fig. 1.28(b). The input resistance of the circuit is $R_1$. The output resistance is zero.

![Inverting low-pass amplifier circuit](image)

#### Example 18

Design an inverting low-pass amplifier circuit which has an input resistance of 10 kΩ, a low-frequency voltage gain of -10, and a pole frequency of 10 kHz.

**Solution.** The circuit diagram of the amplifier is shown in Fig. 1.28(a). For an input resistance of 10 kΩ, we have $R_1 = 10 \text{kΩ}$. The voltage gain transfer function is given by Eq. (1.66). For a low-frequency gain of -10, we have $R_F = 10R_1 = 100 \text{kΩ}$. For a pole frequency of 10 kHz, we have $C_F = 1/2\pi10^4 R_F = 159 \text{pF}$.

A second inverting low-pass amplifier circuit is shown in Fig. 1.29(a). The currents $I_1$, $I_2$, and $I_F$ are given by

$$
I_1 = \frac{V_i}{R_1 + (1/Cs)\|R_2}
$$

(1.67)

$$
I_2 = I_1 \frac{1/Cs}{R_2 + 1/Cs} = I_1 \frac{1}{1 + R_2 Cs}
$$

(1.68)

$$
I_F = \frac{V_o}{R_F}
$$

(1.69)

where it is assumed that the $V_-$ op amp input is at virtual ground and current division has been used for $I_2$. The voltage gain of the circuit can be obtained from the relation $I_2 + I_F = 0$ to obtain

$$
\frac{V_o}{V_i} = -\frac{R_F}{R_1 + R_2} \times \frac{1}{1 + R_1\|R_2 Cs}
$$

(1.70)
This is of the form of a gain constant \(-R_F/(R_1 + R_2)\) multiplied by a low-pass transfer function having a pole time constant \((R_1||R_2)C\). The Bode magnitude plot for the transfer function is given in Fig. 1.29(b).

\[
V_o \over V_i = \frac{1}{1 + (R_1||R_2)Cs} \times \left(1 + \frac{1}{1 + R_F/R_1}\right) \times \frac{1}{1 + RCs}
\]

where voltage division and Eq. (1.10) have been used. This is of the form of a gain constant \(1 + R_F/R_1\) multiplied by the transfer function of a low-pass filter having a pole time constant \(RC\). The Bode magnitude
The output resistance of the circuit is zero. The input impedance is given by

\[ Z_{in} = R + \frac{1}{Cs} = R \times \frac{1 + RCs}{RCs} \]  

This is of the form of a resistor \( R \) multiplied by the reciprocal of a high-pass transfer function.

**Example 20** The non-inverting amplifier of Fig. 1.30(a) is to be designed for a voltage gain of 12. The input low-pass filter is to have a cutoff frequency of 100 kHz. Specify the element values for the circuit.

**Solution.** To meet the cutoff frequency specification, it follows from Eq. (1.72) that \( RC = 1/(2\pi 10^5) \). Either a value for \( R \) or a value for \( C \) must be specified before the other can be calculated. Let \( C = 510 \text{ pF} \). It follows that \( R = 3.12 \text{ k}\Omega \). For a gain of 12, we must have \( 1 + R_F/R_1 = 12 \). If we choose \( R_1 = 1 \text{ k}\Omega \), it follows that \( R_F = 11 \text{ k}\Omega \).

1.8.3 The Non-Inverting Low-Pass Shelving Amplifier

The circuit diagram of a **non-inverting low-pass shelving amplifier** is shown in Fig. 1.31(a). The voltage gain is obtained from Eq. (1.8) by replacing \( R_F \) with \( R_F \parallel (1/C_F) \). It is given by

\[ \frac{V_o}{V_i} = 1 + \frac{R_F \parallel (1/C_F)}{R_1} = \left( 1 + \frac{R_F}{R_1} \right) \frac{1 + R_F \parallel R_1 C_F s}{1 + R_F C_F s} \]  

This is of the form of a gain constant \( 1 + R_F/R_1 \) multiplied by a low-pass shelving transfer function having a pole time constant \( R_F C_F \) and a zero time constant \( (R_F \parallel R_1) C_F \). The Bode magnitude plot for the voltage gain is shown in Fig. 1.31(b). The low-frequency gain is 1 + \( R_F/R_1 \). As frequency is increased, the gain decreases and shelves at unity.

**Example 21** The circuit of Fig. 1.31(a) is to be designed for a low-frequency gain of 2 (a 6 dB boost). The zero frequency in the transfer function is to be 100 Hz. Specify the circuit element values and calculate the frequency at which the voltage gain is 3 dB.

**Solution.** For a low-frequency gain of 2, it follows from Eq. (1.74) that \( 1 + R_F/R_1 = 2 \), which gives \( R_F = R_1 \). For the zero in the transfer function to be at 100 Hz, it follows that \( R_F \parallel R_1 C_F = 1/(2\pi 100) \). If we choose \( C_F = 0.1 \text{ \mu F} \), it follows that \( R_1 = R_F = 31.8 \text{ k}\Omega \). With \( s = j2\pi f \), the voltage gain transfer function can be written

\[ \frac{V_o}{V_i} = \frac{2 + jf/100}{1 + jf/50} \]
1.9 High-Pass Amplifiers

1.9.1 The Inverting High-Pass Amplifier

This section covers several of the many op amp circuits which have a voltage gain that is of the form of high-pass and high-pass shelving transfer functions. Fig. 1.32(a) shows an inverting high-pass amplifier circuit. The voltage gain is obtained from Eq. (1.3) by replacing $R_1$ with $R_1 + 1/(C_1s)$. It is given by

$$\frac{V_o}{V_i} = \frac{-R_F}{R_1 + 1/(C_1s)} = -\frac{R_F}{R_1} \times \frac{R_1C_1s}{1 + R_1C_1s} \quad (1.75)$$

This is of the form of a gain constant $-R_F/R_1$ multiplied by a high-pass transfer function having a pole time constant $R_1C_1$. The Bode magnitude plot for the voltage gain is given in Fig. 1.32(b). The output resistance of the circuit is zero. The input impedance transfer function is given by

$$Z_{in} = R_1 + \frac{1}{C_1s} = R_1 \times \frac{1 + R_1C_1s}{R_3C_1s} \quad (1.76)$$

This is of the form of a resistance $R_1$ multiplied by the reciprocal of a high-pass transfer function.

**Example 22** Design an inverting high-pass amplifier circuit which has a gain of $-10$ and a pole time constant of $500\,\mu$s. The input impedance to the circuit is to be $10\,k\Omega$ or higher. Calculate the lower half-power cutoff frequency of the amplifier.

**Solution.** The circuit is shown in Fig. 1.32(a). The voltage-gain transfer function is given by Eq. (1.75). For the gain specification, we must have $R_F/R_1 = 10$. For the pole time constant specification, we must have $R_1C_1 = 500 \times 10^{-6}$. Because there are three unknowns and only two equations, one of the circuit elements must be specified before the others can be calculated. Eq. (1.76) shows that the lowest value of the input impedance is $R_1$. Thus we must have $R_1 \geq 10\,k\Omega$. If $R_1 \geq 10\,k\Omega$, it follows that $C_1 \leq 0.05\,\mu F$. Let us choose $C_1 = 0.033\,\mu F$. It follows that $R_1 = 15.2\,k\Omega$ and $R_2 = 152\,k\Omega$. The lower half-power cutoff frequency is $f = 1/(2\pi \times 500 \times 10^{-6}) = 318\,Hz$.

At the 3 dB boost frequency, we have $|V_o/V_i|^2 = 1/2$. This condition gives

$$\frac{1 + (f/100)^2}{1 + (f/50)^2} = \frac{1}{2}$$

This can be solved for $f$ to obtain $f = 100/\sqrt{2} = 70.7\,Hz$. 

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**Figure 1.31:** (a) Non-inverting low-pass shelving amplifier. (b) Bode magnitude plot for $|V_o/V_i|$. 
1.9.2 The Non-Inverting High-Pass Amplifier

Figure 1.33(a) shows a non-inverting high-pass amplifier circuit. The voltage gain transfer function is given by

\[
\frac{V_o}{V_i} = \frac{V_x}{V_t} \times \frac{V_o}{V_t} = \frac{R}{R + 1/(Cs)} \left(1 + \frac{R_F}{R_1}\right) = \left(1 + \frac{R_F}{R_1}\right) \times \frac{RCs}{1 + RCs}
\]  

(1.77)

where voltage division and Eq. (1.10) have been used. This is of the form of a gain constant \((1 + \frac{R_F}{R_1})\) multiplied by a single-pole high-pass transfer function having a pole time constant \(RC\). The Bode magnitude plot for the voltage gain is given in Fig. 1.33(b). The output resistance of the circuit is zero. The input impedance transfer function is given by

\[
Z_{in} = R + \frac{1}{Cs} = R \times \frac{1 + RCs}{RCs}
\]

(1.78)

This is of the form of a resistance \(R\) multiplied by the reciprocal of a high-pass transfer function.

Example 23 Design a non-inverting high-pass amplifier which has a gain of 15 and a lower cutoff frequency of 20 Hz. The input resistance to the amplifier is to be 10 kΩ in its passband.

Solution. The circuit is shown in Fig. 1.33(a). In the amplifier passband, \(C\) is a short circuit. To meet the input resistance specification, we must have \(R = 10\) kΩ. The voltage-gain transfer function is given by Eq. (1.77). For a lower half-power cutoff frequency of 20 Hz, we must have \(RC' = 1/(2\pi 20)\). Solution for \(C\) yields \(C = 0.796\) µF. For the gain specification, we must have \(1 + \frac{R_F}{R_1} = 15\) or \(R_1 = R_F/14\). If \(R_F = 56\) kΩ, it follows that \(R_1 = 4\) kΩ.
1.9.3 The Non-Inverting High-Pass Shelving Amplifier

The circuit diagram of a non-inverting high-pass shelving amplifier is shown in Fig. 1.34(a). The voltage gain is given by Eq. (1.10) with $R_1$ replaced by $R_1 + 1/(C_1 s)$. It follows that the gain can be written

$$\frac{V_o}{V_i} = 1 + \frac{R_F}{R_1 + (1/C_1 s)} = \frac{1 + (R_F + R_1) C_1 s}{1 + R_1 C_1 s}$$

(1.79)

This is of the form of a high-pass shelving transfer function having a pole time constant $R_1 C_1$ and a zero time constant $(R_F + R_1) C_1$. The Bode magnitude plot for the voltage gain is shown in Fig. 1.34(b). It can be seen from the figure that the gain at low frequencies is unity. At high frequencies, the gain shelves at $1 + R_F/R_1$.

Example 24 Design a high-pass shelving amplifier which has unity gain at low frequencies, a pole in its transfer function with a time constant of 75 $\mu$s, and a zero with a time constant of 7.5 $\mu$s. What are the pole and zero frequencies and what is the gain at high frequencies?

Solution. The circuit is shown in Fig. 1.34(a). The voltage-gain transfer function is given by Eq. (1.79). For the pole time constant specification, we must have $R_1 C_1 = 7.5 \mu$s. For the zero time constant specification, we must have $(R_F + R_1) C_1 = 75 \mu$s. Because there are three circuit elements and only two equations, we must specify one element in order to calculate the other two. Let $C_1 = 0.001 \mu$F. It follows that $R_1 = 7.5 \text{k\Omega}$ and $R_2 = 75 \text{k\Omega} - R_1 = 67.5 \text{k\Omega}$. The zero frequency is $f_z = 1/(2\pi \times 7.5 \times 10^{-6}) = 2.12 \text{kHz}$. The pole frequency is $f_p = 1/(2\pi \times 7.5 \times 10^{-6}) = 21.2 \text{kHz}$. The gain at high frequencies is $1 + R_F/R_1 = 1 + 67.5/7.5 = 10$.

1.10 The Op Amp as a Comparator

1.10.1 The Inverting Comparator

A comparator is an active circuit element which has two input terminals and one output terminal. The output voltage exhibits two stable states. The output state depends on the relative value of one input voltage compared to the other input voltage. The op amp is often used as a comparator. Fig. 1.35(a) shows the circuit diagram of an op amp used as an inverting comparator. The voltage applied to the non-inverting input is the dc reference voltage $V_{\text{REF}}$. The output voltage is given by

$$v_O = A(V_{\text{REF}} - v_I)$$

(1.80)